

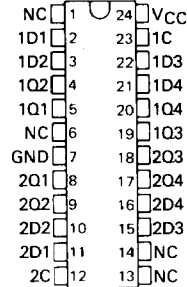
TYPES SN54100, SN74100 8-BIT BISTABLE LATCHES

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- Dependable Texas Instruments Quality and Reliability

SN54100 ... J OR W PACKAGE
SN74100 ... J OR N PACKAGE

(TOP VIEW)



NC—No internal connection

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	Q_0	\bar{Q}_0

H = high level, X = irrelevant
 Q_0 = the level of Q before the high-to-low transition of G

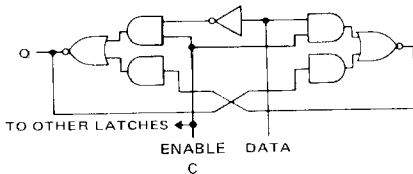
description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was setup at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

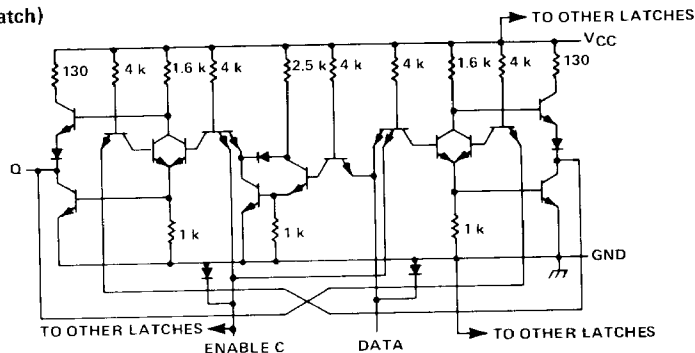
These circuits are completely compatible with all popular TTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Typical power dissipation is 40 milliwatts per latch.

The SN54100 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74100 is characterized for operation from 0°C to 70°C .

logic diagram (each latch)



schematic (each latch)



Resistor values shown are nominal and in ohms.

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TYPES SN54100, SN74100

8-BIT BISTABLE LATCHES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54100	-55°C to 125°C
SN74100	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
 2. This is the voltage between two emitters of a multiple-emitter input transistor. For this circuit, this rating applies between the enable and D inputs of any latch.

recommended operating conditions

	SN54100			SN74100			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	5			5			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT	
V_{IH}	High-level input voltage		2			V	
V_{IL}	Low-level input voltage				0.8	V	
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$	2.4	3.4		V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA	
I_{IH}	High-level input current	D input			80	μ A	
		C input	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		320		
I_{IL}	Low-level input current	D input	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-3.2	mA	
		C input			-12.8		
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	SN54100		-20	-57	mA
			SN74100		-18	-57	
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 3	SN54100		64	92	mA
			SN74100		64	106	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
 ‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

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8-BIT BISTABLE LATCHES**

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, See Note 4	16	30	ns	
t_{PHL}				14	25		
t_{PLH}	C	Q		16	30	ns	
t_{PHL}				7	15		

[†] t_{PLH} = propagation delay time, low-to-high-level output

[†] t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: Load circuits and voltage waveforms are the same as those shown for the '75, '77, 'L75, and 'L77.

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