National Semiconductor

December 1999

LM2413
Monolithic Triple 4 ns CRT Driver

General Description

The LM2413 is an integrated high voltage CRT driver circuit designed for use in high-resolution color monitor applications. The IC contains three high input impedance, wide band amplifiers, which directly drive the RGB cathodes of a CRT. Each channel has its gain internally set to −14 and can drive CRT capacitive loads as well as resistive loads present in other applications, limited only by the package's power dissipation.

The IC is packaged in an industry standard 11 lead TO-220 molded plastic power package. See Thermal Considerations on page 6.

Features

- Rise/Fall times typically 3.7/4.4 with 8 pF load at 40 V_{PP}
- Well matched with LM1282/3 video preamps
- 1V to 5V input range
- Stable with 0–20 pF capacitive loads and inductive peaking networks
- Convenient TO-220 staggered lead package style
- Standard LM240X Family Pinout which is designed for easy PCB layout

Applications

- 1600 x 1200 Displays up to 70 Hz Refresh
- Pixel clock frequencies up to 180 MHz
- Monitors using video blanking

Schematic and Connection Diagrams

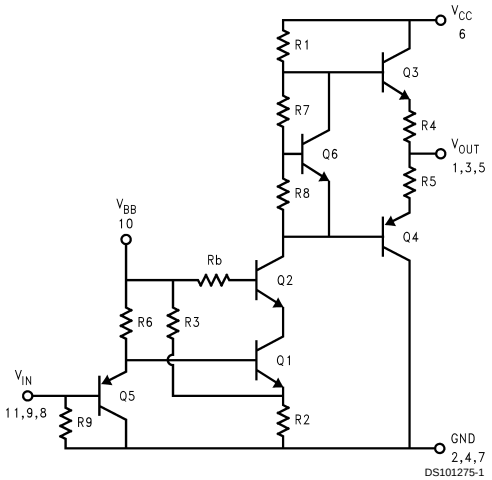
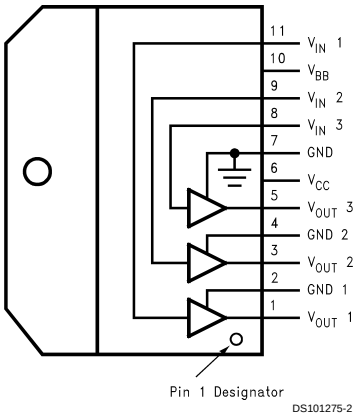


FIGURE 1. Simplified Schematic Diagram (One Channel)



Top View
Order Number LM2413T
See NS Package Number TA11C

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Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	+90V
Bias Voltage, V_{BB}	+16V
Input Voltage, V_{IN}	0V to 6V
Storage Temperature Range, T_{STG}	−65˚C to +150˚C
Lead Temperature (Soldering, ≤10 sec.)	300˚C
ESD Tolerance, Human Body Model	2kV
Machine Model	250V

Operating Ranges (Note 2)

V_{CC}	+60V to +85V
V_{BB}	+10V to +15V
V_{IN}	+1V to +5V
V_{OUT}	+15 to +75V
Case Temperature	−20˚C to +100˚C

Do not operate the part without a heat sink.

Electrical Characteristics (See *Figure 2* for Test Circuit)

Unless otherwise noted: V_{CC} = +80V, V_{BB} = +12V, V_{IN} = +3.3V, No AC Input, C_L = 8pF, T_C = 60˚C

Symbol	Parameter	Conditions	LM2413			Units
			Min	Typ	Max	
I_{CC}	Supply Current	Per Channel, No Output Load	10	16	22	mA
I_{BB}	Bias Current	All three channels	15	25	35	mA
V_{OUT}	DC Output Voltage	V_{IN} = 1.9V	62	65	68	V_{DC}
A_V	DC Voltage Gain		−12	−14	−16	
ΔA_V	Gain Matching	(Note 4)		1.0		dB
LE	Linearity Error	(Notes 4, 5)		3.5		%
t_R	Rise Time (Notes 6, 7)	10% to 90%, 40 V_{PP} Output (1 MHz)		3.7	4.7	ns
t_F	Fall Time (Notes 6, 7)	90% to 10%, 40 V_{PP} Output (1 MHz)		4.4	5.4	ns
OS	Overshoot (Note 6)	(Note 6), 40 V_{PP} Output (1 MHz)		5		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Calculated value from Voltage Gain test on each channel.

Note 5: Linearity Error is the variation in dc gain from V_{IN} = 1.6V to V_{IN} = 5V.

Note 6: Input from signal generator: t_r, t_f < 1 ns.

Note 7: 100% tested in production. These limits are not used to calculate outgoing quality levels.

AC Test Circuit

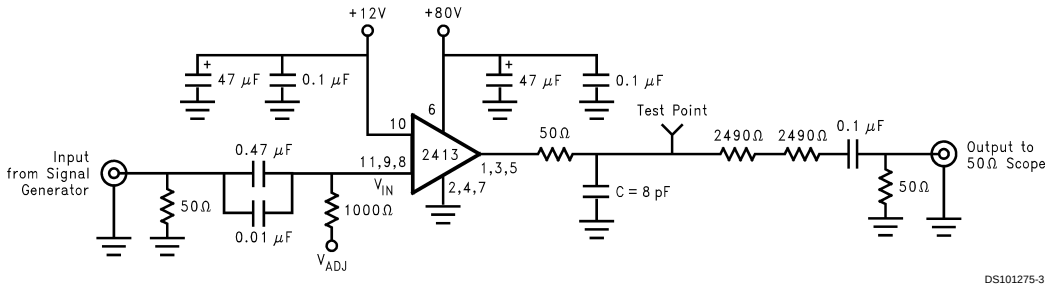

FIGURE 2. Test Circuit (One Channel)

Figure 2 shows a typical test circuit for evaluation of the LM2413. This circuit is designed to allow testing of the LM2413 in a 50Ω environment without the use of an expensive FET probe. The combined resistors of 4950Ω at the output form a 200:1 voltage divider when connected to a 50Ω load. The compensation cap is used to flatten the frequency response of the 200:1 divider.

AC Test Circuit (Continued)

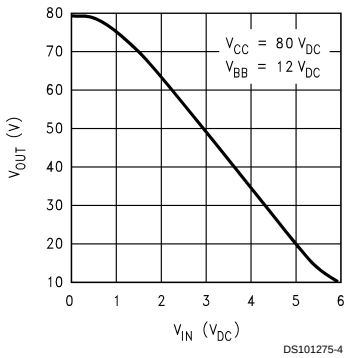

FIGURE 3. V_{IN} vs V_{OUT}

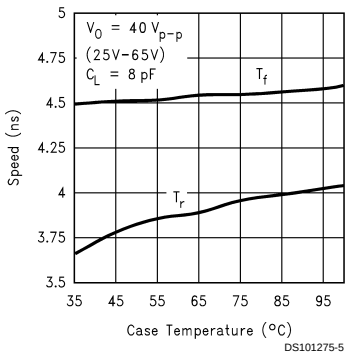

FIGURE 4. Speed vs Temp

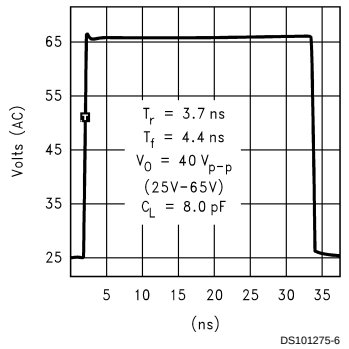

FIGURE 5. Rise/Fall Time

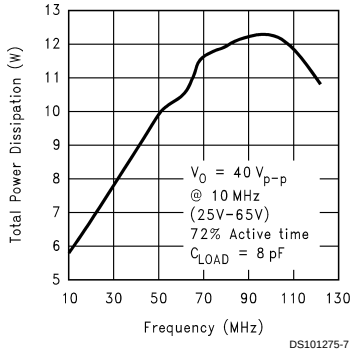

FIGURE 6. Power Dissipation vs Frequency

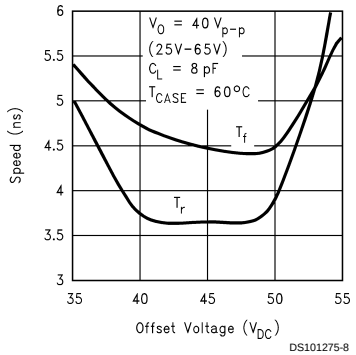

FIGURE 7. Speed vs Offset

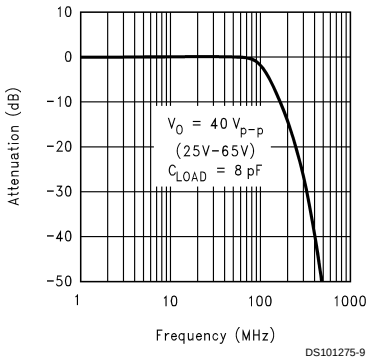

FIGURE 8. Bandwidth

Theory of Operation

The LM2413 is a high voltage monolithic three channel CRT driver suitable for very high resolution display applications, up to 1600 x 1200 at 70 Hz refresh rate. The LM2413 operates using 80V and 12V power supplies. The part is housed in the industry standard 11-lead TO-220 molded plastic power package.

The simplified circuit diagram of one channel of the LM2413 is shown in *Figure 1*. A PNP emitter follower, Q5, provides input buffering. This minimizes the current loading of the video pre-amp. R9 is used to turn on Q5 when there is no input. With Q5 turn on, Q1 will be almost completely off, minimizing the current flow through Q1 and Q2. This will drive the output stage near the V_{CC} rail, minimizing the power dissipation with no inputs. R6 is a pull-up resistor for Q5 and also limits the current flow through Q5. R3 and R2 are used to set the current flow through Q1 and Q2. The ratio of R1 to R2 is used to set the gain of the LM2413. R1, R2, and R3 are all related when calculating the output voltage of the CRT driver. R_b limits the current through the base of Q2. Q1 and Q2 are in a cascode configuration. Q1 is a low voltage and very fast transistor. Q2 is a higher voltage transistor. The cascode configuration gives the equivalent of a very fast and high voltage transistor. The two output transistors, Q3 and Q4, form a class B amplifier output stage. R4 and R5 are used to limit the current through the output stage and set the output impedance of the LM2413. Q6, along with R7 and R8 set the bias current through Q3 and Q4 when there is no change in the signal level. This bias current minimizes the crossover distortion of the output stage. With this bias current the output stage now becomes a class AB amplifier with a crossover distortion much lower than a class B amplifier.

Figure 2 shows a typical test circuit for evaluation of the LM2413. Due to the very wide bandwidth of the LM2413, a specially designed output circuit is used with the required series resistor and C_{LOAD} to emulate the actual application when evaluating the performance of the LM2413 in a 50Ω environment without the use of an expensive FET probe. The combined resistors of 4950Ω at the output form a 200:1 voltage divider when connected to a 50Ω load. The input signal from the generator is ac coupled to the input of the CRT driver. V_{ADJ} input sets the DC operating range of the LM2413.

Application Hints

INTRODUCTION

National Semiconductor (NSC) is committed to providing application information that assists our customers in obtaining the best performance possible from our products. The following information is provided in order to support this commitment. The reader should be aware that the optimization of performance was done using a specific printed circuit board designed at NSC. Variations in performance can be realized due to physical changes in the printed circuit board and the application. Therefore, the designer should know that component value changes may be required in order to optimize performance in a given application. The values shown in this document can be used as a starting point for evaluation purposes. When working with high bandwidth circuits, good layout practices are also critical to achieving maximum performance.

POWER SUPPY BYPASS

Since the LM2413 is a very high bandwidth amplifier, proper power supply bypassing is critical for optimum performance. Improper power supply bypassing can result in large overshoot, ringing and oscillation. A 0.1 µF capacitor should be connected from the supply pin, V_{CC}, to ground, as close to the supply and ground pins as is practical. Additionally, a 10 µF to 100 µF electrolytic capacitor should be connected from the supply pin to ground. The electrolytic capacitor should also be placed reasonably close to the LM2413's supply and ground pins. A 0.1 µF capacitor should be connected from the bias pin, V_{BB}, to ground, as close as is practical to the part.

ARC PROTECTION

During normal CRT operation, internal arcing may occasionally occur. Spark gaps, in the range of 200V, connected from the CRT cathodes to CRT ground will limit the maximum voltage, but to a value that is much higher than allowable on the LM2413. This fast, high voltage, high-energy pulse can damage the LM2413 output stage. The application circuit shown in *Figure 9* is designed to help clamp the voltage at the output of the LM2413 to a safe level. The clamp diodes should have a fast transient response, high peak current rating, low series impedance and low shunt capacitance. FDH400 or equivalent diodes are recommended. D1 and D2 should have short, low impedance connections to V_{CC} and ground respectively. The cathode of D1 should be located very close to a separately decoupled bypass capacitor. The ground connection of the diode and the decoupling capacitor should be very close to the LM2413 ground. This will significantly reduce the high frequency voltage transients that the LM2413 would be subjected to during an arc-over condition. Resistor R2 limits the arc-over current that is seen by the diodes while R1 limits the current into the LM2413 as well as the voltage stress at the outputs of the device. R2 should be a 1/2W solid carbon type resistor. R1 can be a 1/4W metal or carbon film type resistor. Inductor L1 is critical to reduce the inital high frequency voltage levels that the LM2413 would be subjected to during an arc-over. Having large value resistors for R1 and R2 would be desirable, but this has the effect of increasing rise and fall times. The inductor will not only help protect the device but it will also help optimize rise and fall times as well as minimize EMI. For proper arc protection, it is important to not omit any of the arc protection components shown in *Figure 9*. The values of L1 and R1 may need to be adjusted for a particular application. The recommended minimum value for R1 is 110Ω, with L1 = .12 µH.

Application Hints (Continued)

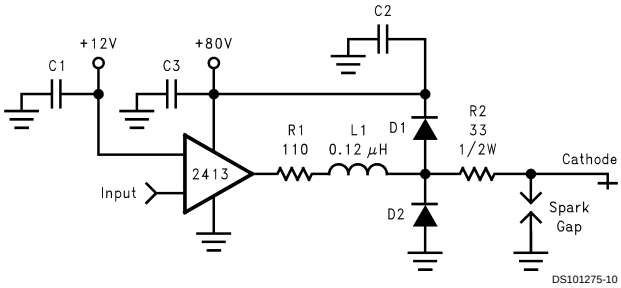

FIGURE 9. One Channel of the LM2413 with the Recommended Arc Protection Circuit

OPTIMIZING TRANSIENT RESPONSE

Referring to *Figure 9*, there are three components (R1, R2 and L1) that can be adjusted to optimize the transient response of the application circuit. Increasing the values of R1 and R2 will slow the circuit down while decreasing overshoot. Increasing the value of L1 will speed up the circuit as well as increase overshoot. It is very important to use inductors with very high self-resonant frequencies, preferably above 300 MHz. The values shown in *Figure 9* can be used as a good starting point for the evaluation of the LM2413.

Effect of Load Capacitance

The output rise and fall times as well as overshoot will vary as the load capacitance varies. The values of the output circuit (R1, R2 and L1 in *Figure 9*) should be chosen based on the nominal load capacitance. Once this is done the performance of the design can be checked by varying the load based on what the expected variation will be during production.

Effect of Offset

Figure 5 shows the variation in rise and fall times when the output offset of the device is varied from 35 to 55 VDC. The rise and fall times show about the same overall variation. The slightly faster rise and fall times are fastest near the center point of 45V, making this the optimum operating point. At the low and high output offset range, the characteristic of rise/fall time is slower due to the saturation of Q3 and Q4. The recovery time of the output transistors takes longer coming out of saturation thus slows down the rise and fall times.

THERMAL CONSIDERATIONS

Figure 4 shows the performance of the LM2413 in the test circuit shown in *Figure 2* as a function of case temperature. *Figure 4* shows that both the rise and fall times of the LM2413 become slightly longer as the case temperature increases from 40˚C to 100˚C. Please note that the LM2413 is **never to be operated over a case temperature of 100˚C.** In addition to exceeding the safe operating temperature, the rise and fall times will typically exceed 3.7/4.4 ns.

Figure 6 shows that total power dissipation of the LM2413 vs. Frequency when all three channels of the device are driving an 8 pF load. Typically the active time is about 72% of the total time for one frame. Worst-case power dissipation is when a one on, one off pixel is displayed over the active time of the video input. This is the condition used to measure the total power dissipation of the LM2413 at different input frequencies. *Figure 6* gives all the information a monitor designed normally needs for worst case power dissipation. However, if the designer wants to calculate the power dissipation for an active time different from 72%, this can be done using the information in *Figure 14*. The recommended input black level voltage is 1.9V. From *Figure 14*, if a 1.9V input is used for the black level, then power dissipation during the inactive video time is 1.95W. This includes both the 80V and 12V supplies.

If the monitor designer chooses to calculate the power dissipation for the LM2413 using an active video time different from 72%, then he needs to use the following steps when using a 1.9V input black level:

1. Multiply the black level power dissipation, 1.95W, by 0.28, the result is 0.6W.
2. Choose the maximum frequency to be used. A typical application would use 90 MHz, or a 180 MHz pixel clock. The power dissipation is 12.4W.
3. Subtract the 0.6W from the power dissipation from *Figure 6*. For 100 MHz this would be 12.4 − 0.6 = 11.8W.
4. Divide the result from step 3 by 0.72. For 90 MHz, the result is 16.4W
5. Multiply the result in 4 by the new active time percentage.
6. Multiply 1.95W by the new inactive time.
7. Add together the results of steps 5 and 6. This is the expected power dissipation for the LM2413 in the designer's application.

The LM2413 case temperature must be maintained below 100˚C. If the maximum expected ambient temperature is 70˚C and the maximum power dissipation is 12.2W (*Figure 6*) then a maximum heat sink thermal resistance can be calculated:

$$R_{TH} = \frac{100°C - 70°C}{12.2W} = 2.46°C/W$$

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This example assumes a capacitive load of 8 pF and no resistive load.

TYPICAL APPLICATION

A typical application of the LM2413 is shown in *Figure 10*. Used in conjunction with an LM1283, a complete video channel from monitor input to CRT cathode can be achieved. Performance is excellent for resolutions up to 1600 x 1200 and pixel clock frequencies at 180 MHz. *Figure 10* is the schematic for the NSC demonstration board that can be used to evaluate the LM1283/2413 combination in a monitor.

Application Hints (Continued)

PC Board Layout Considerations

For optimum performance, an adequate ground plane, isolation between channels, good supply bypassing and minimizing unwanted feedback are necessary. Also, the length of the signal traces from the preamplifier to the LM2413 and from the LM2413 to the CRT cathode should be as short as possible. The red video trace from the LM1283 to the LM2413 input should be considered as short as possible on a PCB layout. If possible, position the pre-amp in such a way where the traces from its output connects to the driver input the most direct and shortest path. The following references are recommended for video board designers:

Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", John Wiley & Sons, New York, 1976.

"Guide to CRT Video Design", National Semiconductor Application Note 861.

"Video Amplifier Design for Computer Monitors", National Semiconductor Application Note 1013.

Pease, Robert A., "Troubleshooting Analog Circuits", Butterworth-Heinemann, 1991.

Because of its high small signal bandwidth, the part may oscillate in a monitor if feedback occurs around the video channel through the chassis wiring. To prevent this, leads to the video amplifier input circuit should be shielded, and input circuit wiring should be spaced as far as possible from output circuit wiring.

NSC Demonstration Board

Figure 11 and *Figure 12* show routing and component placement on the NSC LM1283/2413 demonstration board. The schematic of the board is shown in *Figure 10*. This board provides a good example of a layout that can be used as a guide for future layouts. Note the location of the following components:

- **C79** — V_{CC} bypass capacitor, located very close to pin 6 and ground pins. (*Figure 12*)
- **C55** — V_{BB} bypass capacitor, located close to pin 10 and ground. (*Figure 12*)
- **C75 and C77** — V_{CC} bypass capacitors, near LM2413 and V_{CC} clamp diodes. Very important for arc protection. (*Figure 11*)

The routing of the LM2413 outputs to the CRT is very critical to achieving optimum performance. *Figure 13* shows the routing and component placement from pin 1 to the blue cathode. Note that the components are placed so that they almost line up from the output pin of the LM2413 to the blue cathode pin of the CRT connector. This is done to minimize the length of the video path between these two components. Note also that D14, D15, R29 and D13 are placed to keep the size of the video nodes to a minimum. This minimizes parasitic capacitance in the video path and also enhances the effectiveness of the protection diodes. The anode of protection diode D14 is connected directly to a section of the ground plane that has a short and direct path to the LM2413 ground pins. The cathode of D15 is connected to V_{CC} very close to decoupling capacitor C55 (see *Figure 13*) which is connected to the same section of the ground plane as D14. The diode placement and routing is very important for minimizing the voltage stress on the LM2413 during an arc over event. Lastly, notice that S3 is placed very close to the blue cathode and is tied directly to CRT ground.

Application Hints (Continued)

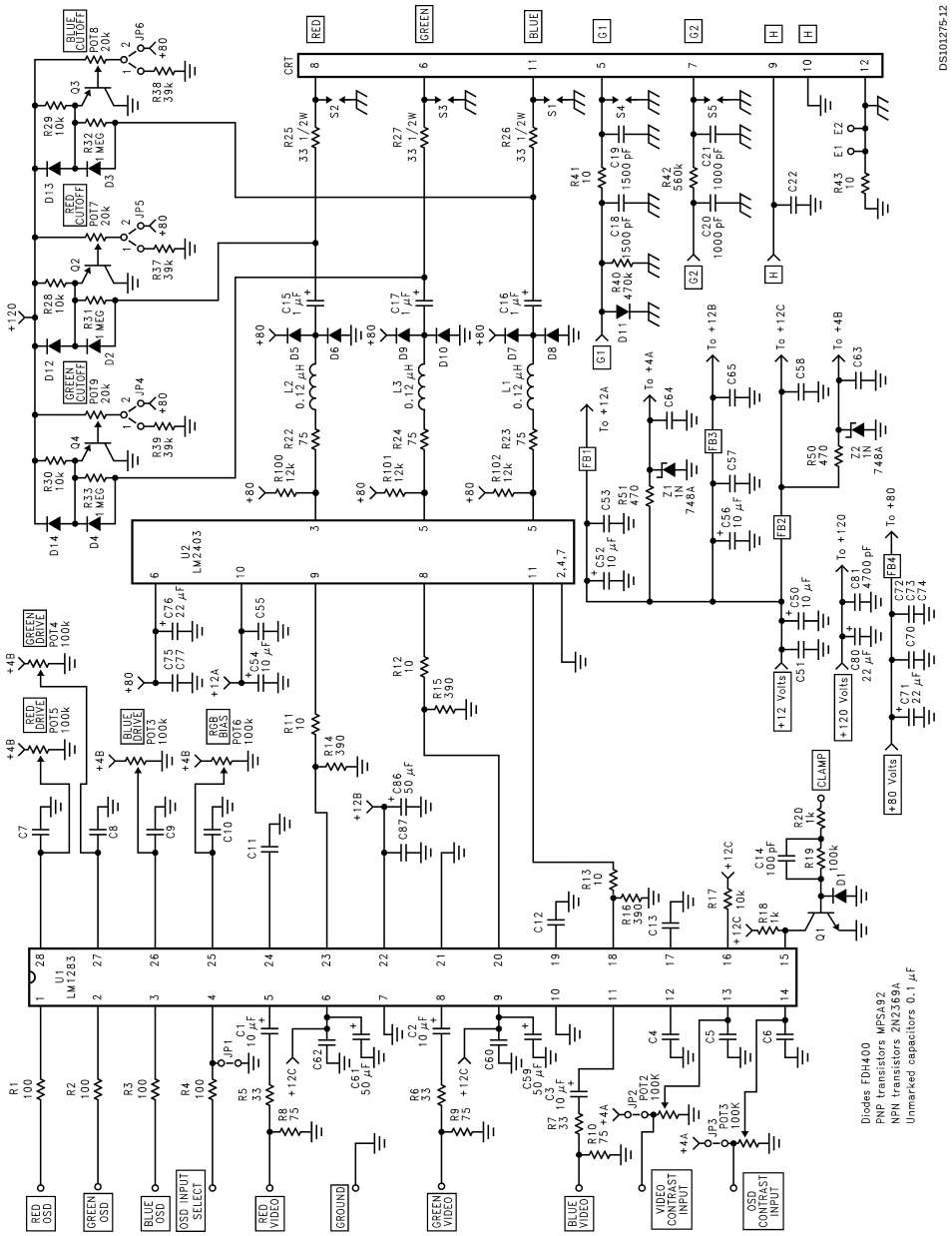

FIGURE 10. National Semiconductor OSD Video Amplier

Application Hints (Continued)

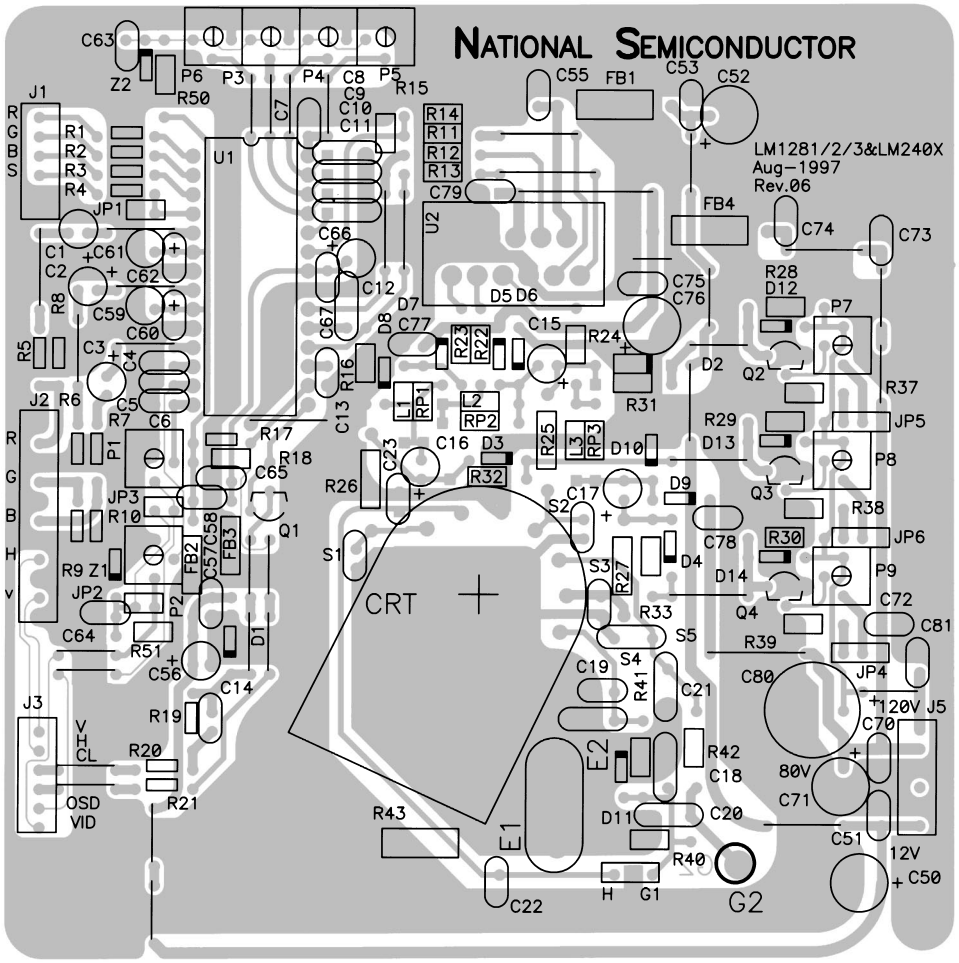

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FIGURE 11. PCB Top Layer

Application Hints (Continued)

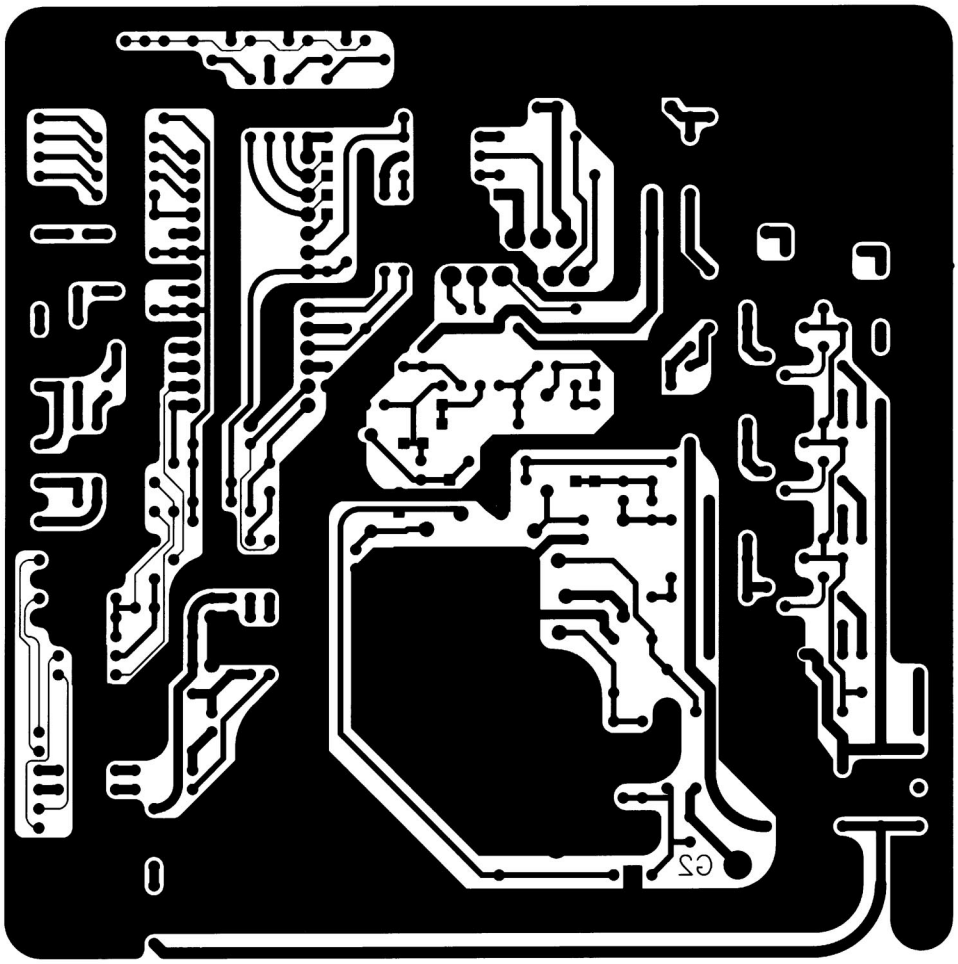

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FIGURE 12. PCB Bottom Layer

Application Hints (Continued)

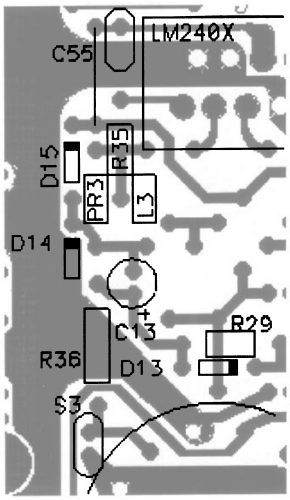

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FIGURE 13. PCB CRT Driver, Blue Channel Output

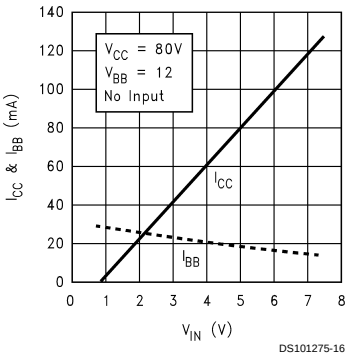

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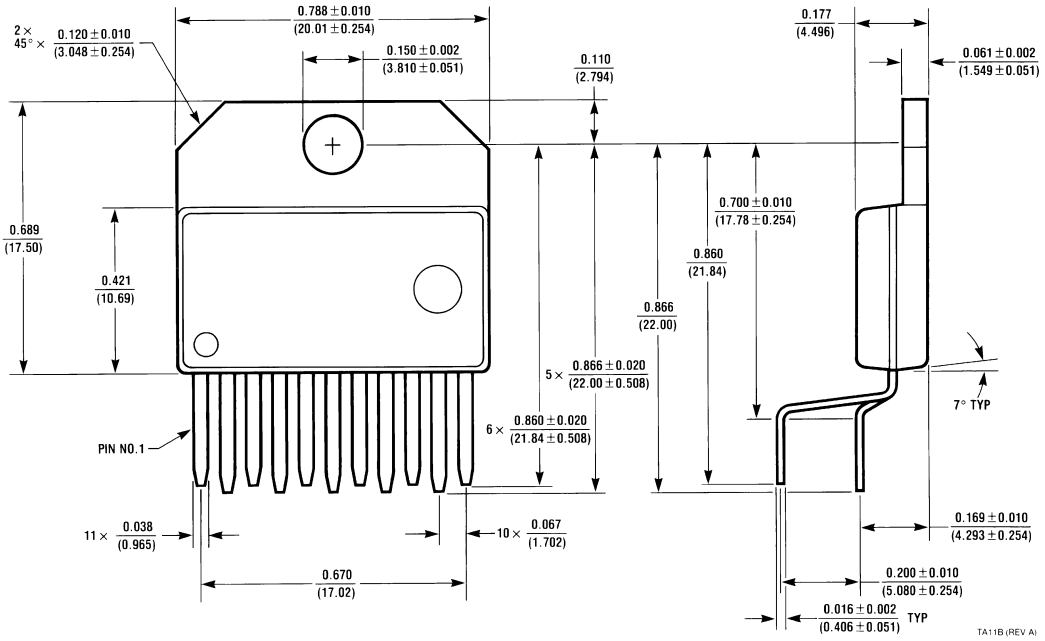
FIGURE 14. I_{CC} and I_{BB} vs V_{IN}

Physical Dimensions inches (millimeters) unless otherwise noted



NS Package Number TA11B

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